Design of High gain Boost Converter for Standalone applications

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Abstract: The main problem is renewable energy sources like solar pv arrays is they are operating at very low voltage which is insufficient for many standalone applications where voltage gain requirement high. For these type of applications high efficiency, high voltage gain and reduction in switch voltage, component count, ripple in input current are the priority features. To handle this issue a high voltage gain boost converter is presented. The converter with the combination of coupled inductors and voltage-doubler structure is proposed to achieve high voltage gain. Voltage-doubler structure is kept in the secondary winding of the coupled inductor which decrease the diode voltage stress. This converter output is fed as input to a neutral point clamped inverter and is connected to the 3-phase induction motor. There is a implementation of maximum power point tracking (MPPT) perturbation observance algorithm for a photo voltaic system so as to extract maximum power from the solar cell, also to calculate the reference speed to the induction motor due to change in irradiance and temperature of PV cell.

Keywords: High voltage gain, Coupled inductor, Active clamp circuit, neutral point clamped inverter, V/F control

1. INTRODUCTION

Traditional methods (thermal plants, diesel generators, and nuclear plants) of power production is deteriorating the environment because of generation by these methods produce dangerous waste and gases.

Solar plants are the optimal option for power generation either in huge or low amounts. Solar plants are installed using a set of multiple photovoltaic planes which generate direct current (DC) power. The output voltage of solar PV sources is typically unregulated and is insufficient for the most of the applications. As a result, applications like UPS and micro-grids have emerged [1-5]. Utilising them for a wide variety of applications such as grid-connected systems and stand-alone applications becomes highly challenging due to the high voltage boosting requirement.

Operation of converter topologies at large duty cycles increases the losses in parasitic resistances of components[3]. One of the possible solution is cascade connection of several boost converters, but it gives the lower efficiency and greater control complexity. The techniques reported to attain high voltage gain with non isolated structures comprise switched inductors[6], switched capacitors, voltage doubler and bootstrap capacitors [7-10]. Most important technique for getting high voltage gain is using coupled inductors[9],[10]. Reduced component count is achieved by some coupled inductor based circuits [11],[12].

Buck converter which is discontinuous input current converter need another filter for reducing electro magnetic interference increases the number of components Input current with negligible ripple can be achieved by inductor circuits but the drawback is they have low voltage gain[13],[14]. By combining the zero-ripple boost cell and coupled inductor gives input current with negligible ripple and also gives high voltage gain,[15],[16].

This paper represents the improved features of boost converter topology by integrating voltage doubler structure which safeguard the output diode from high voltage stress, gives high voltage gain and eliminates the resonance between the output diode
junction capacitor and leakage inductance. Hence switching loss is reduced and implemented for standalone PV applications.

2. STANDALONE APPLICATION WITH INDUCTION MOTOR

The proposed boost converter is fed as input to a neutral point clamped inverter and is connected to three phase induction motor. An implementation of maximum power point tracking perturbance observer algorithm for a PV system so as to extract maximum power from the solar arrays during unfavourable condition, also to calculate the reference speed to the induction motor due to change in irradiance and temperature of PV cell. Following Figure 1 depict the complete block diagram of the system connected to 3-Ø induction motor.

![Figure 1. Block diagram of entire standalone application system](image)

3. High gain and efficient dc-dc converter

Solar PV systems have a modest efficiency (about 14–28 percent). As a result, an efficient power conversion system is required. The high gain converter (boost) topology with maximum gain comprising input inductor \(L_{in}\), coupled inductors with magnetising inductance \(L_{mag}\), intermediate capacitors \(C_{aux}\), output capacitor \(C_{out}\), main and auxiliary switches \(S_{max}\) and \(S_{aux}\), is shown in Figure 1. For efficient operation of the converter circuit, clamp circuit is made up of \(V_{in}\), while the voltage doubler circuit is made up of the capacitor \(C_{aux}\) and diodes \(D_{aux}\). The proposed circuit's steady-state analysis with the continuous conduction having coupled inductors' coupling coefficient, \(k = \frac{L_{mag}}{L_{mag} + L_{l}}\), where \(L_{l}\) denotes leakage inductance, The turns ratio is given by \(n = \frac{L_{mag}}{L_{l}}\).

![Figure 2. High gain converter (boost dc-dc)](image)

Figure 2 shows the various operating modes in CCM (Continuous Conduction Mode).
Figure 3. Modes I, II & III operation of the Novel converter (boost dc-dc)

In mode-I, as in Figure 3, \( S_{\text{aux}} \) is turned off at \( t = t_0 \). The negative current \( i_2 \) discharges \( C_r \) to zero from \( (V_{\text{out}} + V_{\text{aux}} - V_{\text{CL}}) \), and the diode \( D_{\text{aux}} \) begins to conduct. As a result, zero voltage is applied across \( S_{\text{main}} \) and \( V_{\text{mag}} \), the voltage across \( L_{\text{mag}} \) is \( (V_{\text{CL}} - V_{\text{CL}})/u \) and thus the current \( i_4 \) is expressed as

\[
i_4(t) = \frac{V_{\text{out}} - V_{\text{aux}} - (V_{\text{CL}} - V_{\text{CL}})}{L_{\text{mag}}}(t - t_0) + i_4(0)
\]

Since, \( i_{\text{aux}} \) \( \leq 0 \), \( D_{\text{aux}} \) is conducting.

In mode-II, at \( t = t_0 \), \( S_{\text{main}} \) is ON while \( D_{\text{aux}} \) is conducting under ZVS conditions. diode \( D_{\text{aux}} \) is turned off.

In mode-III, \( i_{\text{aux}} \) charges the capacitor at the junction of \( D_{\text{aux}} \) to \( V_{\text{aux}} \) and discharges the junction capacitor of \( D_{\text{aux}} \) to zero in a small period of time. When \( D_{\text{aux}} \) begins to conduct, the voltage across the inductance \( L_{\text{aux}} \) changes to \( \frac{V_{\text{aux}} - V_{\text{aux}} - V_{\text{CL}}}{u} \), and the current \( i_4 \) is calculated as

\[
i_4(t) = \frac{V_{\text{aux}} - V_{\text{aux}} - V_{\text{aux}}}{L_{\text{aux}}}(t - t_0) + i_4(0)
\]

The currents flowing through main switch \( i_{\text{main}} \) and diode \( D_{\text{aux}} \), are \( i_4 \) and \( (i_4 - i_{\text{aux}})/\eta \), respectively.

![Figure 3](image)

Figure 4. Modes IV, V & VI operation of the Novel converter (boost dc-dc)

From Figure 4, the mode IV, At \( t = t_3 \), \( S_{\text{main}} \) is OFF and the leakage current \( i_4 \) rapidly charges the capacitor at the junction \( D_{\text{aux}} \), from ‘0’ to \( (V_{\text{aux}} + V_{\text{aux}} - V_{\text{CL}}) \), causing the \( D_{\text{aux}} \) to be operating. The slope of \( i_{\text{aux}} \) remains the constant, and the series resonant circuit is formed by leakage inductance \( L_{\text{aux}} \) and capacitor \( C_{\text{aux}} \), with expressions

\[
L_{\text{aux}} \frac{dV_{\text{aux}}}{dt} + V_{\text{aux}} = 0.
\]

\[
i_4 = C_{\text{aux}} \frac{dV_{\text{aux}}}{dt}
\]

The conduction of diode \( D_{\text{aux}} \) makes zero voltage across \( S_{\text{aux}} \).

In Mode-V, to achieve ZVS, turn on the auxiliary switch \( S_{\text{aux}} \) at \( t = t_3 \). The magnetizing current \( i_{\text{mag}} \), current \( i_4 \), and capacitor \( C_{\text{aux}} \), voltage \( V_{\text{aux}} \) expressions will be the same as in mode-4. The diode \( D_{\text{aux}} \) is kept in conduction by the negative \( i_4 \).

In Mode-VI at \( t = t_6 \), the current \( i_{\text{aux}} \) reverses direction and diode \( D_{\text{aux}} \) ceases to conduct. Current \( i_{\text{aux}} \) charges capacitor at the junction of \( D_{\text{aux}} \), from zero to \( V_{\text{aux}} \) and discharges, that of \( D_{\text{aux}} \) to zero. The magnetizing current slope is changes to \( \frac{V_{\text{aux}} - V_{\text{aux}}}{u_{\text{aux}}} \), respectively.

2.1 Analysis of the High Gain Converter:

The converter's mathematical analysis is required in order to design the components that would be employed in its construction. All of the converter's components are considered to be ideal.
During on condition $DTs$ in mode III
\[ V_{L_{\text{on}g}} = \frac{V_{\text{in}}}{n} \cdot T_{\text{on}} \] (6)

During on condition $DTs$ in mode VI
\[ V_{L_{\text{on}g}} = \frac{V_{\text{in}}}{n} \cdot T_{\text{on}} \] (7)

From the equations (6) & (7)
\[ V_{\text{in}} = \frac{V_{\text{out}}}{n} 
\]
\[ \frac{V_{\text{out}}}{n} \cdot DT_{\text{on}} + \frac{V_{\text{in}}}{n} \cdot T_{\text{on}} \cdot (1-D) T_{\text{on}} = 0 \]
\[ V_{\text{out}} = V_{\text{in}} + V_{\text{on}} \] (8)

Voltage across leakage inductance during OFF condition in mode VI is given by
\[ V_{L_{\text{off}}} = \frac{V_{\text{out}} - V_{\text{in}}}{1-D} \] (9)

Substituting $V_{\text{in}}$, $V_{\text{out}}$ and $V_{\text{on}}$ values in equation (8)
\[ V_{\text{on}} = (V_{\text{out}} - V_{\text{in}}) \]
\[ V_{L_{\text{off}}} = \frac{V_{\text{out}} - V_{\text{in}}}{1-D} \] (10)

Voltage across leakage inductance during ON condition in mode III is given by
\[ V_{L_{\text{on}g}} = \left( -V_{L_{\text{on}g}} + V_{\text{out}} - V_{\text{in}} \right) \] (12)

Voltage across leakage inductance during OFF condition in mode VI is given by
\[ V_{L_{\text{off}}} = \left( V_{\text{out}} - V_{\text{in}} \right) \] (13)

Applying volt–second balance on inductors
\[ \left( -V_{L_{\text{on}g}} + V_{\text{out}} - V_{\text{in}} \right) d + \left( -V_{L_{\text{off}}} + V_{\text{in}} \right) (1-d) = 0 \]
\[ V_{\text{max}} = \frac{V_{\text{out}} - V_{\text{in}} - V_{\text{off}} d}{(1-d)} \] (14)

From equation (9), $V_{\text{in}} = V_{\text{out}} - V_{\text{on}}$
Substitute $V_{\text{in}}$ value in equation (14)
\[ V_{\text{max}} = \frac{V_{\text{out}} - V_{\text{off}} - V_{\text{on}} d}{(1-d)} \] (15)

Voltage gain is written as
\[ A_{v} = \frac{V_{\text{out}}}{V_{\text{in}}} \] (16)

3.2 Design procedure:

\[ D_{0102} \text{ voltage equal to } V_{\text{out}} \cdot \frac{D_{0102}}{D_{0102}} \text{, equals load current, } i_{\text{load}} \]

As a result, the diode’s current stress can be calculated as
\[ 0.5i_{\text{diode}}(1-d) = 0.5i_{\text{diode}} d = i_{\text{on}} \]
\[ i_{\text{diode}} = \frac{i_{\text{on}}}{1-d} \] (17)

Voltage across switches $S_{\text{on}}$ and $S_{\text{off}}$ are given by
\[ V_{\text{on}} = \frac{V_{\text{on}}}{1-d} \] (18)

The maximum current stress is experienced by both switches at $t = t_{0}$
\[ i_{\text{diode}} = \frac{2n i_{\text{on}} - n i_{\text{diode}} V_{\text{diode}} d}{2L_{\text{diode}}} \] (19)
The value of \( d \) is chosen to limit voltage across to no more than twice the input voltage, \( V_{in} \). Any other criterion for selecting \( d \), on the other hand, will sufficient to begin the design process.

\[
\frac{n}{L_{mag}} = \frac{V_{in}}{2\Delta v_{out}}
\]  
(20)

\[
\Delta v = \frac{\Delta v_{CL} + \Delta v_{out}}{2}
\]  
(21)

net voltage ripple, \( \Delta v \), is \( \Delta v = (\Delta v_{CL} + \Delta v_{out}) \).

Flux linkage is given by

\[
\phi = \frac{1}{2}\Delta v_{out} \frac{L_{in}}{(1-d)}
\]  
(22)

For voltage ripples \( \Delta v_{CL} \), \( \Delta v_{G2} \), and \( \Delta v_{out} \), the required value of capacitances \( C_{G2} \), and \( C_{out} \), are given a

\[
C_{G2} = \frac{(n-1)\Delta v_{CL}}{2\Delta v_{G2}}
\]  
(24)

\[
C_{out} = \frac{6n(1-a)\Delta v_{out}}{\Delta v_{out}}
\]  
(26)

For \( V_{in} = 48V \), \( V_{out} = 400V \), \( n = 4 \):

from equations (20) and (21): \( \frac{L_{mag}}{2\Delta v_{out}} \leq 2\frac{V_{in}}{(1-d)} \leq 2\frac{V_{out}}{(1-d)} \); \( d = 0.5 \); \( n = \frac{V_{out}}{V_{in}} = \frac{400}{48} = 8.33 \); \( n = 4 \)

\[
L_{mag} = 180 \mu H
\]

\[
C_{G2} = 2 \mu F
\]

\[
C_{out} = 5 \mu F
\]

With converter parameters as per Table 1, voltages across and current through capacitors, diodes and inductance are obtained as

<table>
<thead>
<tr>
<th>TABLE 1 CONVERTER SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input dc voltage</td>
</tr>
<tr>
<td>Output voltage</td>
</tr>
<tr>
<td>Turns ratio of coupled inductor</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>Coupled inductor</td>
</tr>
<tr>
<td>Input inductor</td>
</tr>
<tr>
<td>Output power</td>
</tr>
</tbody>
</table>

Voltage gain \( A_v = \frac{V_{out}}{V_{in}} \) we get \( A_v = 8 \); \( V_{out} = \frac{bk}{1-d} \), \( V_{out} = 400V \)

\[
V_{CL} = 52V; V_{G2} = (kn-1) V_{in}, V_{G2} = 144V, V_{G2} = \frac{V_{out} - V_{CL}}{1-d}, V_{G2} = 52V
\]

Ripple and RMS expression:

\[
\Delta v_{out} = \frac{\Delta v_{out}}{\phi} = \frac{\Delta v_{out}}{\frac{1}{L_{mag}}} = \frac{\Delta v_{out}}{\phi} = \frac{\Delta v_{out}}{\frac{1}{L_{mag}}}
\]

18.41A: \( I_{ramp(\phi)} = I_{ramp(\phi)} \sqrt{B + \left( \frac{B}{3} \right)} \frac{\Delta v_{out}}{\phi} = 8.99A \)

\[
I_{G2} = \frac{8.89A}{1.2} \sqrt{\frac{1 - B}{3}} = 1.2A
\]

For the same parameters \( (V_{in} = 48V, F_{sw} = 100 kHz, L=60\mu H, C = 5\mu F) \), Table 3 shows the comparision of designed high gain boost converter with conventional boost converter.
2. Three level neutral point clamped inverter

Figure 9 depicts the three phase NPC circuit. This inverter is a modified form of a two-level inverter topology, with two new semiconductor switches added per phase. DC bus voltage which actually is split into two parts using the capacitor link. So, the midpoint of this two capacitors is being accessed by the converter. So there are no two separate DC sources, but the dc source is split into two parts using two capacitors and the midpoint.[17-24] The clamping diode restricts the voltage stress across the switches to the voltage value. $\frac{V_{dc}}{2}$ is the voltage across the capacitor. The switching states of a three-level inverter are shown in Table 1.

![Fig 5 circuit diagram of Three level neutral point clamped inverter](image)

In order to understand the operation of the circuit in detail, we take only one phase of the converter and analyze it in detail[18]. So that we can also understand the other phases are identical in operation.

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Switching sequence for phase A</th>
<th>Inverter terminal voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>on on off off</td>
<td>$+\frac{V_{dc}}{2}$</td>
</tr>
<tr>
<td>0</td>
<td>off on off off</td>
<td>0</td>
</tr>
<tr>
<td>-1</td>
<td>off off on on</td>
<td>$-\frac{V_{dc}}{2}$</td>
</tr>
</tbody>
</table>

4. RESULTS AND DISCUSSION

The converter is analyzed in simulation with MATLAB/Simulink environment.
The above Figure 5 shows the complete simulation model of the system with detailed descripted parameters in Table 3.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>5kHz</td>
</tr>
<tr>
<td>Couple inductor turns ratio</td>
<td>4</td>
</tr>
<tr>
<td>Module peak power</td>
<td>245.025W</td>
</tr>
<tr>
<td>Open circuit module voltage(V_{oc})</td>
<td>48.8V</td>
</tr>
<tr>
<td>Short circuit module current(I_{sc})</td>
<td>6.43A</td>
</tr>
<tr>
<td>MPP voltage of module(V_{mp})</td>
<td>40.5V</td>
</tr>
<tr>
<td>MPP current of module(i_{mp})</td>
<td>6.05A</td>
</tr>
<tr>
<td>MPP voltage of array(V_{mp})</td>
<td>40.5V</td>
</tr>
<tr>
<td>MPP current of array(I_{mp})</td>
<td>6.05A</td>
</tr>
</tbody>
</table>

The waveform of current, voltage supplied by the PV array is shown in below Figure 7.

Figure 7 PV voltage current waveforms

Outputs of switch voltage, Magnetizing current, output Current, voltage through diode and voltages of clamped capacitors during various operational modes are shown in Figure 8 and Figure 9 Figure 10 and Figure 11.

Figure 8 a) Waveform of auxillary voltage  b) Efficiency of novel boost converter
The outputs of Neutral point clamped inverter are shown in Figure 11 and speed torque curves of induction motor are shown in Figure 12.

The parameters corresponding to change in irradiance is tabulated and presented in Table 5.
The operation of the high gain converter is compared with boost converter in terms of parameters given as per Table 5. But in practical application circuits, the inductor in conventional boost converter will not be perfectly inductive with zero internal resistance due to which the maximum operating duty ratio of the traditional boost converter will be restricted to (0.4-0.6). As a result, we can't operate at 0.9 duty cycle practically, and thus can't obtain large voltage gain using the traditional converter. The switch drop and switching losses obtained are high. So it causes high loss switching. Hence it is clear that the novel topology is superior in performance.

### TABLE 5 COMPARISON WITH CONVENTIONAL BOOST CONVERTER

<table>
<thead>
<tr>
<th></th>
<th>Boost converter d=0.9, Ron=0.068ohms</th>
<th>Proposed converter d=0.5, Ron=0.008ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>( \frac{V_b}{V_a} = \frac{1}{d} ) = 480v</td>
<td>( \frac{V_b}{V_a} = \frac{1}{d} ) = 480v</td>
</tr>
<tr>
<td>Current through inductor</td>
<td>( \frac{1}{2} d L_s = 7.2A )</td>
<td>( \frac{1}{2} d L_s = 4.8A )</td>
</tr>
<tr>
<td>Switch voltage drop</td>
<td>( \frac{d V_s}{d t} = \frac{480V}{1-0.5} = 100v )</td>
<td>( \frac{d V_s}{d t} = \frac{480V}{1-0.5} = 100v )</td>
</tr>
<tr>
<td>Leakage energy</td>
<td>( \frac{d}{d t} \left( \frac{d V_a}{d t} \right)^2 = 0.46w )</td>
<td>( \frac{d}{d t} \left( \frac{d V_a}{d t} \right)^2 = 0.005w )</td>
</tr>
</tbody>
</table>

Novel converter with large gain implemented for low and medium-voltage source applications. High gain is obtained at lower duty cycles with minimum switching is obtained. The efficiency of dc-dc converter at full load is obtained as 94-97 %. Output voltage, diode currents and voltages, capacitor voltages are calculated. The converter is fed to a three phase phase neutral point clamped inverter, which is then connected to the three phase induction motor. Induction motor speed control is done by V/F control. PV source with Perturb observer mppt algorithm is used for getting the reference speed for the V/F control. Reference voltage generated by V/F control is given to the PWM generator. With respect to the reference voltage by comparing reference voltage with two carrier waves switching pulses are generated which are given to inverter and all the required characteristics are observed. Waveforms of output voltage diode currents and voltages, voltage and current across main and auxiliary switches of high gain dc-dc converter are observed. Speed torques characteristics of three phase induction motor are

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**5. CONCLUSION**

Novel converter with large gain implemented for low and medium-voltage source applications. High gain is obtained at lower duty cycles with minimum switching is obtained. The efficiency of dc-dc converter at full load is obtained as 94-97 %. Output voltage, diode currents and voltages, capacitor voltages are calculated. The converter is fed to a three phase phase neutral point clamped inverter, which is then connected to the three phase induction motor. Induction motor speed control is done by V/F control. PV source with Perturb observer mppt algorithm is used for getting the reference speed for the V/F control. Reference voltage generated by V/F control is given to the PWM generator. With respect to the reference voltage by comparing reference voltage with two carrier waves switching pulses are generated which are given to inverter and all the required characteristics are observed. Waveforms of output voltage diode currents and voltages, voltage and current across main and auxiliary switches of high gain dc-dc converter are observed. Speed torques characteristics of three phase induction motor are
observed. The proposed converter's performance is verified in a simulation environment, and the findings are presented.

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