GDI BASED LOW POWER HIGH SPEED 4 BIT SHIFT REGISTER

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ABSTRACT

In electronic devices are moving drastically towards high-speed design feature. The traditional D-flip flop is no longer suitable for designing shift registers because of its low-speed performance. Many different types of shift registers, such as Universal Shift registers, Serial In Serial Out, Serial In Parallel Out, Parallel In Parallel Out and Parallel In Serial Out have been developed. Also, there are many low-power shift registers design techniques that have been proposed.

A shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected. Flip-flop consumes power and constitute load on the clock distribution. To achieve the high performance in universal shift register, flip-flops play the important role. Pass-Transistor Logic, A popular and widely-used, which attempts to reduce the number of transistors required to implement logic by allowing the primary inputs to drive gate terminals as well as source/drain terminals. And reduce the overall power area as well as delay.

This paper enumerates the efficient design and analysis of 4-bit shift registers using D flip- flop. It is designed by utilizing less number of transistors. This results in drastic improvement of power, area & delay. In this D flip-flop based on GDI technique is designed and newly designed D flip-flop is used in order to design shift registers. The shift registers used here provides comparatively less power dissipation, area & delay. Design and simulation of shift registers has been carried out using Microwind tool.

Keywords: Shift Registers, GDI technique

1. introduction:

A register is a group of flip-flops that is required to store binary information. Each flip-flop is a binary cell which is capable of storing one bit of information. An n bit register is composed by n flip-flops and is capable of storing n bits. In addition to flip-flops, register may have combinational gates that perform certain data processing tasks to control that when the new information is transferred into the register.

Registers are broadly classified into buffer or storage registers and shift registers. Storage registers have provision to store the data and making it available when required where as shift registers are capable to store the data and shifting its binary information either to right or to the left. In shift registers the flip-flops are connected in cascade configuration, with input of one flip-flop connected to the input of next flip flop. All flip-flops are triggered by a common clock pulse which enables the shift operation in register.

1.1 Shift Registers:

If the register is capable of shifting bits either towards right hand side or towards left hand side is known as **shift register**. An 'N' bit shift register contains 'N' flip-flops. Following are the four types of shift registers based on applying inputs and accessing of outputs.

- Serial In Serial Out shift register
- Serial In Parallel Out shift register
- Parallel In Serial Out shift register
- Parallel In Parallel Out shift register

Serial In − Serial Out shift register :

The shift register, which allows serial input and produces serial output is known as Serial In – Serial Out (SISO) shift register. The block diagram of 4-bit SISO shift register is shown in the following figure.

This block diagram consists of four D flip-flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip-flops are synchronous with each other since, the same clock signal is applied to each one.

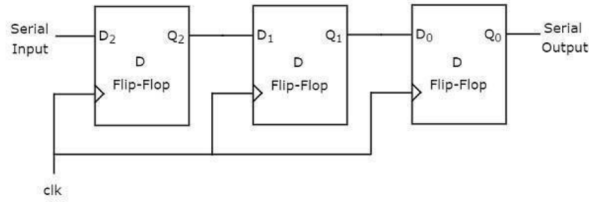

Fig 1: Serial In – Serial Out shift register

In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as serial output.

Serial in-Parallel out shift register:

The shift register, which allows serial input and produces parallel output is known as Serial In-Parallel Out (SIPO) shift register. The block diagram of 4-bit SIPO is shown in the following figure.

This circuit consists of four D flip- flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip- flops are synchronous with each other since, the same clock signal is applied to each one.

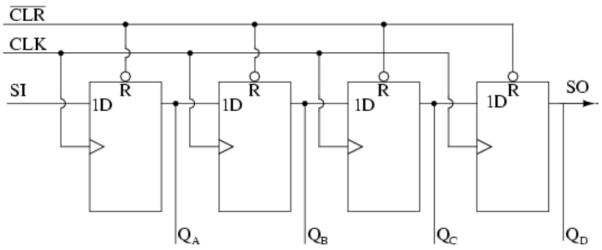

Fig 2: Serial In-Parallel Out shift register

In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. In this case, we can access the outputs of each D flip-flop in parallel. So, we will get parallel **o**utputs from this shift register.

Parallel In-Serial Out shift register:

The shift register, which allows parallel input and produces serial output is known as Parallel In − Serial Out (PISO) shift register. The **block diagram** of 4-bit PISO shift register is shown in the following figure.

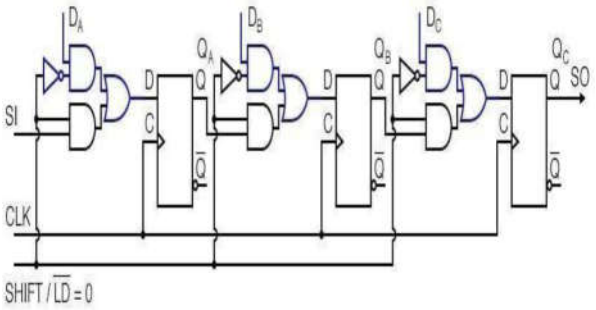

Fig 3: Parallel In - Serial Out shift register

This circuit consists of four D flip- flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip- flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we will get the serial output from the right most D flip-flop.

Parallel In-Parallel Out shift register:

The shift register, which allows parallel input and produces parallel output is known as Parallel In − Parallel Out (PIPO) shift register. The block diagram of 4-bit PIPO shift register is shown in the following figure.

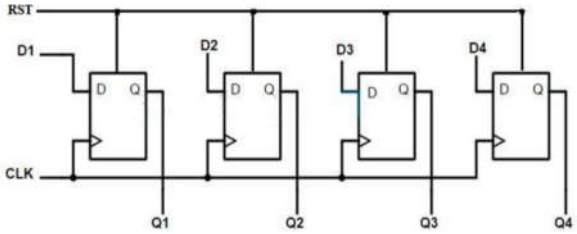

Fig 4: Parallel In - Parallel Out shift register

This circuit consists of four D flip- flops, which are cascaded. That means, output of one D flip-flop is connected as the input of next D flip-flop. All these flip- flops are synchronous with each other since, the same clock signal is applied to each one.

In this shift register, we can apply the parallel inputs to each D flip-flop by making Preset Enable to 1. We can apply the parallel inputs through preset or clear. These two are asynchronous inputs. That means, the flip-flops produce the corresponding outputs, based on the values of asynchronous inputs. In this case, the effect of outputs is independent of clock transition. So, we will get the parallel outputs from each D flip-flop.

2. GDI Technique:

GDI (Gate Diffusion Input) is the latest technology for designing of VLSI circuits. It is considered as more efficient technique as it consumes less power, less area, and it also has lower complexity of designing. This technique is most predominant for designing circuits in MOSFET technology. This technique allows reducing power consumption, delay, and area of digital circuit while maintaining the low complexity of logic design. It could show better results in terms as speed as well. The Gate diffusion Input (GDI) cell contains four terminals G node (the common gate input of NMOS and PMOS), P node (the outer diffusion node of the PMOS), N node (the outer diffusion node of the NMOS), D node (the common diffusion node of both PMOS AND NMOS).-P, N, and D

nodes may be used as either input or output nodes, depending on the circuit structure.

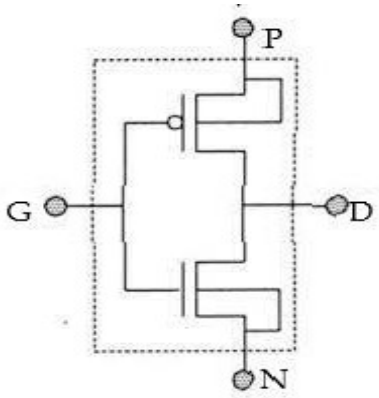

Fig 5: Basic GDI cell

2.1 Our Proposed Technique:

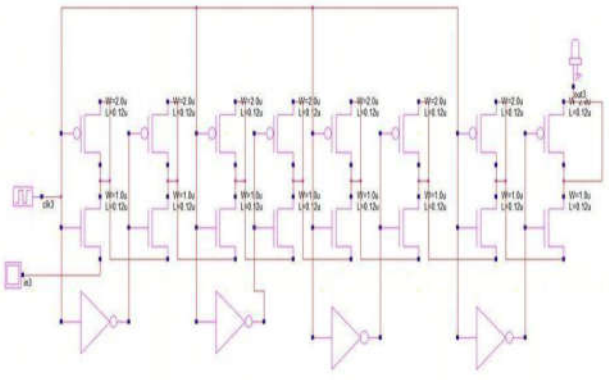

Fig 6: Serial In-Serial Out shift register

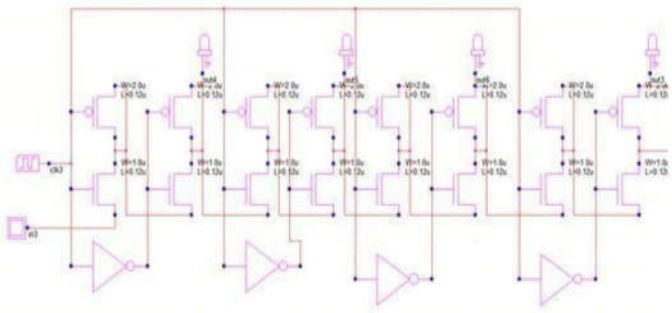

Fig 7: Serial In-Parallel Out shift register

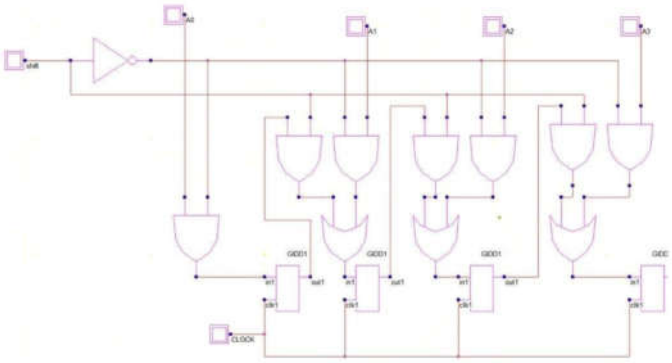

Fig 8: Parallel In-Serial Out shift register

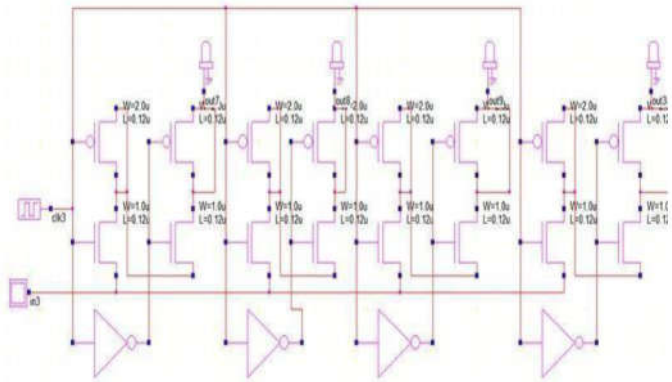

Fig 9: Parallel In-Parallel Out shift register

3. Stimulation Results:

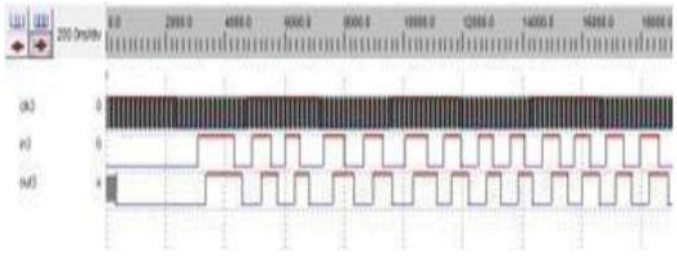

Fig 10: Simulation output of SISO

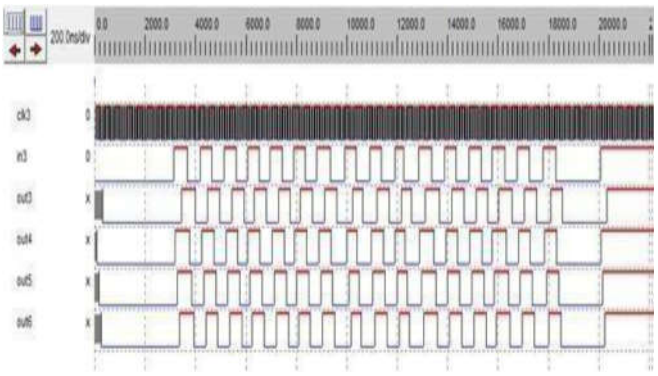

Figure11: Simulation output of SIPO

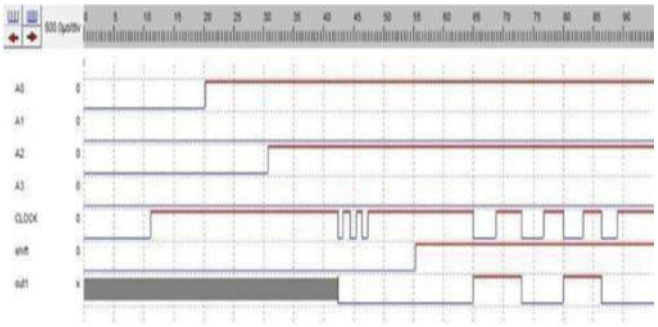

Fig 12: Simulation output of PISO

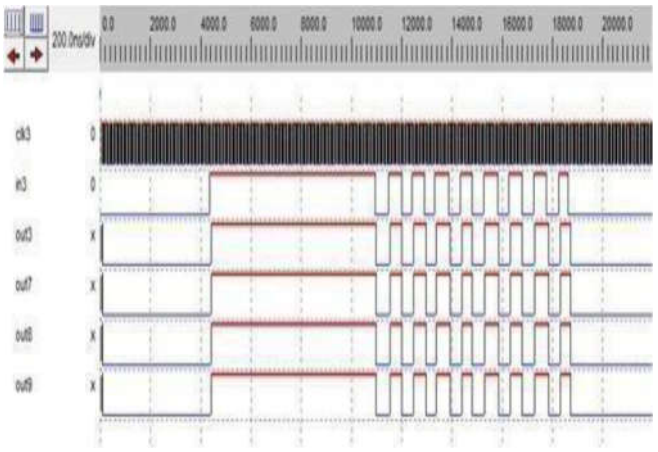

Figure13: Simulation output of PIPO

4. Power consumption:

Technologies	SISO	SIPO	PISO	PIPO
0.8µm	0.804 mW	2.109 mW	2.645 mw	3.430 mW
0.12 µm	3.662 µW	8.019 µW	8.703 µW	16.820 µW

5. Conclusion:

Thus 4-bit shift register is designed based on the GDI technique which predominantly decreases the power dissipation, area and delay. The transistor count is also minimized and this design can perform faster. Shift Register shoes better performance and results compared to normal designs.

When compare with 0.12 µm technology 0.8µm technology gives better performance interms of power dissipation that is a very less power is consumed in 0.8µm technology.

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