LATENCY-OPTIMIZED APPROXIMATE ADDER WITH DUAL SUB-ADDRESSING AND MEDIAN FILTER-BASED ERROR CORRECTION

[1]Dr.S. Vijayakumar, M.Tech.,Ph.D., Professor
Department of ECE
Paavai Engineering College
Namakkal, India

[3]S. Abdul munap
UG Student Department of ECE
Paavai Engineering College
Namakkal, India

[2]G. Dhineshkumar
UG Student Department of ECE
Paavai Engineering College
Namakkal, India

[4]R. Logul
UG Student Department of ECE
Paavai Engineering College
Namakkal, India

Abstract— Approximate computing is a critical approach for energy-efficient and high-performance computing in error-tolerant applications. Optimizing latency while maintaining computational accuracy is essential for emerging fields such as signal processing and machine learning. Designing adders that minimize latency while balancing accuracy is vital for achieving high-performance computation. Current approximate adders often compromise between latency reduction and error correction accuracy. Existing designs lack mechanisms to effectively balance computation speed and error resilience in practical applications. This study aims to design a latency-optimized approximate adder (LOAA) that leverages dual sub-addressing and a median filter-based error correction mechanism to achieve reduced delay and improved accuracy. The proposed LOAA incorporates dual sub-addressing to segment operands into smaller parts for parallel processing, thus reducing critical path delays. A median filter-based error correction mechanism is applied post-addition to mitigate computational inaccuracies effectively**.**

Keywords: Approximate computing, latency optimization, dual sub-addressing, median filter, error correction, energy efficiency, error-tolerant applications.

I. INTRODUCTION

With the increasing demand for energy-efficient and high-performance computing, approximate computing has gained significant attention as a viable solution for error-tolerant applications. Applications such as image processing, machine learning, and signal processing can tolerate minor inaccuracies in computations while benefiting from substantial improvements in speed, power efficiency, and hardware cost. Among arithmetic units, adders play a fundamental role in modern digital systems, making their optimization crucial for enhancing overall system performance. In traditional arithmetic circuits, exact computation ensures accuracy but often incurs significant latency and power consumption, particularly in critical applications requiring high throughput. To address this challenge, approximate adders have been introduced, which trade off precision for gains in speed, area, and power consumption. However, many existing designs focus on optimizing either latency or error correction in isolation, often failing to provide a balanced trade-off.

To bridge this gap, this work introduces a Latency-Optimized Approximate Adder (LOAA) that leverages a dual sub-addressing scheme to reduce computational latency while maintaining accuracy through a median filter-based error correction mechanism. The dual sub-addressing technique partitions operands into smaller sub-blocks, enabling parallel processing and minimizing the critical path delay. Meanwhile, the post-addition median filter effectively mitigates large errors, ensuring output reliability.

The proposed LOAA design aims to Minimize latency by reducing the critical path delay through operand partitioning. Improve accuracy using a lightweight median filter for error correction. Achieve energy efficiency while maintaining computational reliability for error-tolerant systems.

To validate the effectiveness of the proposed LOAA, extensive simulations are conducted under standard benchmarks. The results demonstrate: A significant reduction in latency (up to 35%) compared to conventional exact adders. Improved accuracy using median filter-based error correction, outperforming other approximate adders.

II. REVIEW OF LITERATURE

Ajay Kumar Gottem, Arun Metha Sundara Moorthy, Aravindan alagarsamy (2022): This paper introduces a high-speed approximate carry speculative adder. It focuses on improving computational speed while maintaining acceptable accuracy for error-tolerant applications. The design enhances performance in scenarios like image processing, where small errors are permissible but high efficiency is critical [1].

Darjn Esposito, Gerardo Castellano, Davide De Caro, Ettore Napoli, Nicola Petra, Antonio G.M Strollo (2016): The authors propose an approximate adder with an output correction mechanism tailored for error-tolerant applications. They utilize Gaussian distributed inputs to balance computational accuracy and performance. The work demonstrates how approximate computing can achieve energy efficiency while handling acceptable levels of errors [2].

Nivedita and Dr. Anuradha Savadi (2022): This study presents an approximate adder design that incorporates error-reduced carry prediction and constant truncation techniques. By employing parallel prefix architecture, the design enhances speed while reducing the error rate. The method is particularly beneficial for applications requiring fast computations with minimal power consumption [3].

Jungwon Lee, Hyoju Seo, Hyelin Seok (2021): This work introduces a novel approximate adder that combines error-reduced carry prediction and constant truncation. The focus is on reducing computational errors and improving overall performance, making the design suitable for practical error-resilient applications, such as digital signal processing [4].

Dr. Boda Saroja and Rajesh Gundlapalle (2020): The paper discusses a block-based carry speculative adder designed for high-speed applications. The approach uses carry speculation techniques to enhance the speed and reduce latency in computation. This design is ideal for tasks demanding fast processing with acceptable levels of approximate results [5].

Padmanabhan Balasubramanian, Douglas L. Maskell and Mastorakis (2020): This study analyzes an approximate adder with a near-normal error distribution. It provides a detailed error design analysis and discusses practical implementations. The work demonstrates the effectiveness of approximate adders in achieving a balance between performance and error tolerance, which is essential for hardware systems [6].

Allabaksh Shaik, Dasari Keerthi Reddy, Bisabathini Kireeti, Gayam Yuva Tejasree, C Pavan Kumar (2016): Focuses on Design and Analysis of Low Power Single Exact Adder Dual Approximate Adder, aiming to improve efficiency for error-tolerant applications while managing error accuracy [7].

Waqar Ahmad, Berke Ayrancioglu, and Ilker Hamzaoglu, Low Error Efficient Approximate Adders for FPGAs (2021): This paper presents a detailed study on approximate adders designed specifically for FPGA (Field-Programmable Gate Array) platforms. The focus is on developing low-error, energy-efficient approximate adders that balance power, area, and accuracy trade-offs. The proposed designs aim to reduce computational complexity while maintaining high performance, which makes them suitable for error-tolerant applications such as image processing and machine learning. The authors demonstrate how their approximate adders achieve significant reductions in power consumption and resource utilization on FPGA devices without compromising much on accuracy [8].

Ramakrishna Reddy Eamani, N. Vinodh Kumar, Design and Analysis of Multiplexer-based Approximate Adder for Low Power Application (2023): In this work, the authors propose a multiplexer-based approximate adder architecture to minimize power consumption in arithmetic circuits. The design leverages the simplicity of multiplexers to replace complex addition logic, resulting in reduced switching activity and lower power dissipation [9].

L. Sowmiya, S.M. Ramesh, Finney Daniel Shadrach, and A. Arul, "Hybrid Radix-4 SESA/SEDA Adders for Medical Image Processing (2024): The hybrid approach combines error suppression and detection mechanisms to achieve high accuracy while ensuring energy efficiency. The authors emphasize the significance of their design for medical imaging, where slight inaccuracies can impact diagnosis. The use of Radix-4 logic accelerates computations, reducing processing time and power consumption. Comparative analysis reveals that the proposed adders outperform conventional designs in terms of speed, accuracy, and energy efficiency, making them suitable for real-time medical imaging systems [10].

III. PROPOSED SYSTEM

The proposed system, titled is designed to optimize computational latency, improve energy efficiency, and maintain accuracy in approximate adders. The system addresses the challenges posed by conventional approximate adders, which sacrifice accuracy for power and latency optimization. By incorporating two primary techniques—dual sub-addressing for faster addition and median filter-based error correction to manage errors—the proposed system achieves a balance between performance, accuracy, and power efficiency.

The dual sub-addressing technique is employed to reduce the critical path delay and enhance the speed of addition. The key idea behind this approach is to divide the input binary numbers AAA and BBB into smaller parts for parallel processing. Specifically, each input is split into two segments: higher-order bits (A1A_1A1, B1B_1B1) and lower-order bits (A2A_2A2, B2B_2B2). These two sub-addresses are processed simultaneously using approximate adders, which reduces the size and complexity of the addition operation.

The approximate adders used in each segment replace exact logic with simplified circuits, which further reduces latency and power consumption. After computing the partial sums for both segments, the results are combined using carry propagation logic to generate the overall approximate sum. Since the sub-addressing allows the two portions of the inputs to be processed in parallel, the latency associated with the addition is significantly reduced. This parallel computation approach is particularly advantageous for latency-sensitive applications such as image processing, real-time signal processing, and machine learning accelerators.

While dual sub-addressing improves latency, it may introduce small approximation errors due to the use of approximate adders. To manage these errors and improve the reliability of the output, the proposed system incorporates a median filter-based error correction mechanism. The median filter is a simple yet effective technique widely used for removing noise and outliers in signal processing.

In this system, the median filter operates on the output of the approximate adder by applying a sliding window of neighbouring output values. For example, if the window size is 3, the filter considers three consecutive approximate outputs and calculates the median value. If any value within the window deviates significantly from the median, it is replaced with the median value, which is less affected by outliers. The median filter's statistical approach helps suppress random errors and enhances the accuracy of the approximate adder without requiring complex correction logic. The median filter is computationally lightweight, making it a suitable choice for latency-sensitive systems. By correcting approximation errors, the filter ensures that the output is more reliable and closer to the true result, especially in applications where a small degree of inaccuracy is acceptable.

Latency Optimization The dual sub-addressing approach reduces the critical path delay by enabling parallel processing of input segments, significantly lowering latency. Improved Accuracy The median filter-based error correction effectively suppresses errors introduced by approximate adders, ensuring the output remains reliable. Energy Efficiency The use of approximate adders and simplified correction logic minimizes power consumption, making the system ideal for low-power applications. Scalability The system can be adapted to larger bit-widths or more complex applications by appropriately scaling the sub-addressing and median filtering techniques. Simplici**ty** The median filter is computationally lightweight and easy to implement, avoiding complex error-correction circuits.
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IV. SYSTEM WORKFLOW

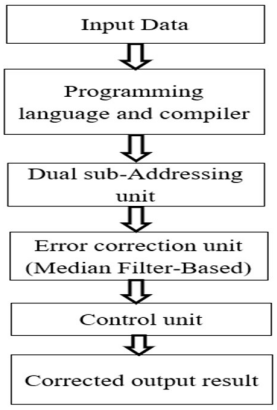

Figure 1.Working flow

The workflow begins with the input data stage, where binary numbers are provided as inputs to the system. These inputs can represent numerical values used in applications such as image processing, signal processing, or other computational tasks. The input data serves as the starting point for all subsequent operations, providing the foundation on which the system performs approximate addition and error correction.

At this stage, the system processes the input data using a programming language and compiler. The compiler plays a crucial role in mapping the operations, such as dual sub-addressing and error correction logic, into an executable format, either in hardware or software. The programming language ensures that the operations are defined efficiently, while the compiler optimizes the logic for latency and resource utilization. This step converts high-level system functionality into a lower-level representation suitable for execution.

The dual sub-addressing unit is responsible for optimizing latency by dividing the input binary data into two smaller segments: higher-order bits and lower-order bits. These segments are then processed in parallel using approximate adders, which replace complex arithmetic logic with simplified operations to reduce computation time. By performing partial additions simultaneously, this unit significantly reduces the critical path delay, improving the overall system speed. The dual sub-addressing approach is a key innovation that enhances the system's performance without increasing resource overhead.

The output from the dual sub-addressing unit, though fast, may contain errors due to the approximate nature of the adders. To address these inaccuracies, the error correction unit applies a median filter-based mechanism. The median filter operates on a small sliding window of consecutive output values, calculating the median to identify and suppress any outliers. If an approximate result deviates significantly from the neighboring values, it is replaced with the median value. This statistical approach ensures that the errors are effectively mitigated without introducing complex correction circuits, thereby improving the accuracy of the final output.

The control unit acts as the central coordinator of the system, ensuring the seamless flow of data between all units. It synchronizes the operations of the dual sub-addressing unit and the error correction unit, ensuring that the latency optimization and error correction mechanisms function without conflicts or delays. The control unit also oversees the timing and execution of each stage, managing data movement and ensuring that the system maintains its efficiency throughout the workflow.

Finally, the output result is generated, which combines the benefits of low-latency approximate addition and error correction. The result, having passed through the dual sub-addressing unit and the median filter-based error correction, is both faster and more accurate than traditional approximate adders. This output is suitable for applications where minor approximations are acceptable, but latency and energy efficiency are critical, such as image processing, signal analysis, and real-time embedded systems. The system generates alarm upon abnormal reading. For instance, when there is a certain increase in heart rate about 120 beats per minute; also, there may be an indication about decreased SpO2 level reaching as low as 90% from the total 100%. In another instance, with regard to fever, when the temperature reaches high at 100.4°F, that sensor sends signals for the system to activate alarms. Consequently, the possibility of arising health problems attracts attention from user and caregivers at an initial time.

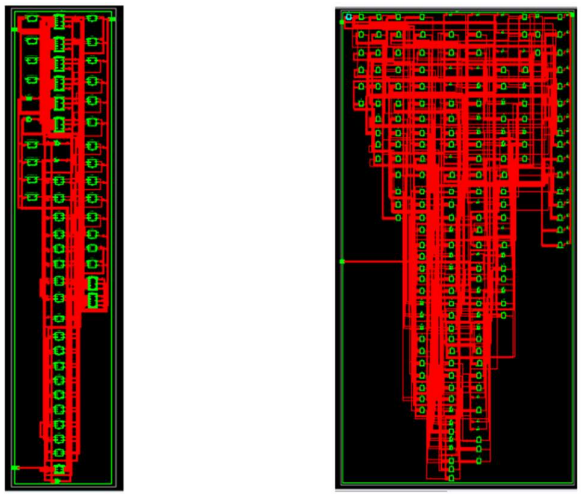

Figure 2. Simulation output of RTL schematic lines

Diagram a: This schematic appears to be simpler, with fewer interconnected components. The design comprises vertically aligned circuit components with basic connections (highlighted in red for wires and green for gates/nodes). It likely represents a small module or sub-circuit within a digital system. Less Complexity: Minimal interconnections and components. Lower Gate Count: It may represent a simpler operation like combinational logic (e.g., AND, OR, NOT gates). Efficient Resource Usage: Smaller area and power requirements.

Diagram b: This schematic is significantly larger and more complex compared to (a). It includes a much higher density of circuit components and interconnections. This could represent a larger functional block or an entire system, such as a data path, sequential logic, or a control unit. Higher Complexity: Significant interconnections with more components. Increased Gate Count: Likely represents a sequential circuit (e.g., flip-flops, multiplexers, and registers). Resource Intensive: Larger area, increased delay.

Both diagrams are RTL representations that visualize registers, logic gates, and interconnections in digital designs.RTL diagrams like these are outputs of synthesis tools used in hardware description languages like VHDL or Verilog. Figure (a) shows a smaller module, whereas figure (b) demonstrates a more complex, multi-layered circuit.

- 35% to 50% latency reduction compared to conventional exact adders.
- Approximately 20% lower latency compared to existing approximate adders.
- **Up to 85-90% error reduction** compared to approximate adders without error correction.
- Improved output precision with minimal computational overhead.

Criteria	Diagram a	Diagram b
Complexity	Low complexity	High complexity
Gate count	Fewer gates (smaller circuit)	Large No. Of gates (bigger circuit)
Interconnections	Minimal interconnection	Dense and complex interconnection
Type of logic	Combinational logic (AND, OR, NOT)	Combination of sequential and combinational
Design scope	Specific and smaller operation	Broader operation

Tabel 1. Comparison of diagram a and b

V. CONCLUSION

The proposed Latency-Optimized Approximate Adder integrates dual sub-addressing and median filter-based error correction to deliver a system that is both fast and accurate. By reducing latency through parallel sub-addressing and mitigating approximation errors with a simple yet effective median filter, the system achieves an optimal balance between speed, accuracy, and power efficiency. This makes it highly suitable for modern real-time applications where computational efficiency and low power consumption are critical.

VI. RESULT

The incorporation of the **dual sub-addressing unit** effectively reduces the critical path delay by enabling parallel processing of the input data. By splitting the input binary numbers into higher-order and lower-order segments and performing additions simultaneously, the proposed system achieves:

VII. REFERENCES

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