OPTIMIZING CIRCUIT PERFORMANCE AND POWER THROUGH ERROR AWARE CLOCK CONTROL

[1] Dr. S. Vijayakumar., MTech., Ph.D., Professor, Paavai Engineering College, Pachal, Namakkal
[2] M Nisha, Student, Paavai Engineering College, Pachal, Namakkal
[3] V G P Reethi, Student, Paavai Engineering College, Pachal, Namakkal
[4] P Varshini, Student, Paavai Engineering College, Pachal, Namakkal
[5] P Yogashree, Student, Paavai Engineering College, Pachal, Namakkal

Abstract: This paper introduces a new way in semiconductors, as semiconductors technology continues to scale down, the demand for high-performance and energy-efficient circuits becomes increasingly critical. In this context, timing errors, often caused by variations in pressure, voltage, and temperature (PVT), pose significant challenges to circuit reliability and efficiency. Traditional Design approaches typically add timing margins to prevent such errors, which can lead to suboptimal performance and excessive power consumption. By presenting a novel methodology for improving circuit performance and power efficiency, this work contributes to the broader goals of sustainable technology development and innovation.

Index terms: Circuit Design, Timing Errors, Process, Voltage and Temperature (PVT), Timing Margin, Advanced Scaling, Performance Improvement, Power Consumption Reduction.

I INTRODUCTION

The evolution of modern electronics has driven the Need for circuits that can operate at high speeds while maintaining low power consumption. However, as integrated circuits shrink to nanometer scales, timing errors caused by variations in process, voltage, and temperature (PVT) have become a major challenge. A wide- voltage-range half-path timing error-detection system with a 9-transistor transition-detector in 40-nm CMOS with initialize circuit monitor[1]. These errors not only compromise circuit reliability but also necessitate the use of conservative design margins, which can hinder performance and increase power consumption.

In response to these challenges, timing errors-aware clock control has emerged as a cutting-edge approach that leverages real-time feedback mechanisms to optimize circuit operation. Timing error tolerance in small core designs for SoC applications with resilient timing [4]. Unlike traditional methods that rely on static timing analysis, this technique dynamically adjusts the clock signal to mitigate timing errors. Short-Path Padding for Resilient Circuits, Dynamic TG-SPP Control [2] [17]. By allowing circuits to function closer to their critical path delays, timing error-aware clock control enhances performance without overdesigning for worst- case scenarios.

This approach integrates seamlessly with advanced clock gating and dynamic voltage-frequency scaling (DVFS), to achieve further power savings. By coupling timing error detection with adaptive clock adjustments, circuits can operate more efficiently, reducing unnecessary energy consumption while maintaining high reliability. A time-borrowing method for performance improvement of low-power digital circuits prone to variations[8]. The ability to balance performance, power, and reliability in this manner is especially critical in domains such as medical electronics, automative system, and the internet of things (IOT), where the constraints are stringent.

II RELATED STUDY

The proposed method was compared with other major timing-error-tolerant methods by considering hardware overhead and performance, as summarized. Timing Error Detection for Near-Threshold Operation, Energy-Efficient Timing Error Correction for ASICs [9].

The hardware overhead is analyzed by evaluating the area of transistors. The overhead based on the area of transistors is derived as

Area overhead = Nr / Ns

Where Nr is the area of transistors required for timing error tolerance and Ns is the area of transistors required for data storage.

The area of transistors was evaluated by referring to the criteria channel size of transistors in 90-nm standards cells. The area of transistors required for timing error tolerance is calculated based on additional CMOS transistors except for the original flip-flop in one stage. The area of transistors required for data storage is calculated with flip-flop of the original circuit in one stage. For comparison between existing methods and the proposed system, we determined that

the hardware composition in one stage plays a major role in error tolerance. For instance, the basic hardware composition for timing-error recovery, which affects the setup time of the next stage. Current-based error detection and correction scheme for PVT variation in 40-nm ARM cortex-R4 processor[5]. Thus, the control hardware that deals with the timing error tolerance in several stages is excluded in our comparison.

When the systems are compared by the area of transistors the area overhead of the proposed system is the lowest among all SEU hardening methods that can detect and correct the error immediately.

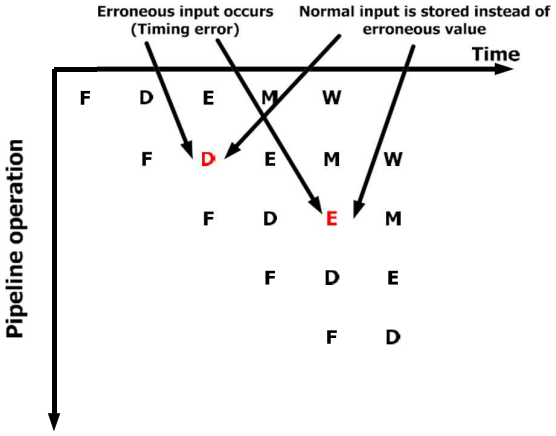


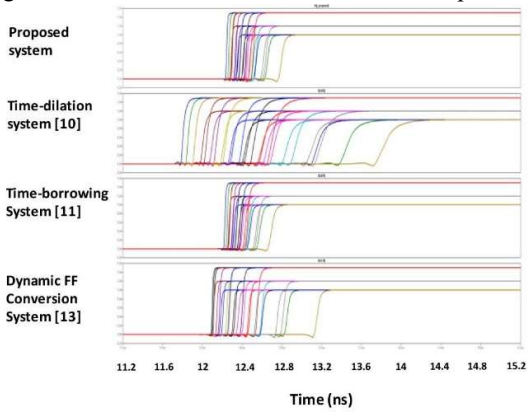
Fig. 1. Timing-error recovery in pipeline stages (F: fetch, D; decode, E: execute, M: memory, and W: write back).

For instance, in dynamic flip-flop conversion system, the circuit is composed in figure1 of one timing violation predictor, one data-arrival detector, and the original flip-flop. The dynamic flip-flop conversion system has 430% hardware overhead since the additional hardware consists of 68 transistors robust system[25]. Design of Light-Weight Timing Error Detection and Correction Circuits for Energy-Efficient Near-Threshold Voltage[21]. Clock Tree Synthesis with Multibit Flip-Flops, Dynamic Placement and Routing for MBFF-Based Clock Trees[6].

Compared with the power overhead of the other methods, the proposed systems required less power overhead than other existing methods that can detect and correct instantly except error-detection systems. The time-redundant systems can only detect an error. The area overhead is calculated by assuming that the proposed system in one stage consists of one transistor detector, one master clock generator, and one flip-flop. The additional hardware consists of transition are required for additional hardware. The other two error-detection systems optimized the circuit for error detection, so they require a small amount.

To show performance improvement, we implemented our system on five benchmark circuits in the International Test Conference'99(ITC'99). The maximum allowable frequency (MAF) is used to evaluate the performance of our proposed system and other timing-error-tolerant systems that can detect and correct the error instantly. For comparison, time-redundant system, time-dilation system, time-borrowing system, and dynamic flip-flop conversion system with benchmarks of EEG Signal Classification for Seizure Detection [3]. The benchmark circuits are synthesized, and the critical paths are reported. By performing simulation with original circuits and information of the critical path, the frequency is increased by a certain percentage of MAF of the original circuits. Meanwhile, if a timing violation occurs, each method is applied to the FF which reports timing violation.

Fig. 2. Simulated waveforms of the final output of



each system with PVT variations

Overall, even though the hardware overhead of the proposedsystem is lower than that of the existing methods, the proposed system still has high performance. Used in dynamic phase-locked lock(PLL) based monitoring algorithm input device operating conditions, phase noise[24]. Our proposed system is designed to operate the targeted function, but it is not yet designed with consideration for possible glitches. Since the glitch occurs for a short duration, the glitch can be removed by adjusting CMOS parameters[20][7]. Delay- Insensitive Supervisory Control Algorithm Input: Discrete- event system model, bounded communication delay, and system constraints, Predictive Control with Delay Compensation Algorithm Input: Event occurrence times, estimated communication delays, and control system constraints[23].

For instance, if the width or the length of transistors in the "transition detector" is changed, the glitch can be removedby adjusting the rising or falling slope. With this technique, signal "Er" could be delayed, which can result in a little lower performance. On the other way, the glitch can be removed by changing the circuit of the "transition detector," which could cause larger hardware overhead. To address the

glitch, we can adopt one of the methods that are stated above in further study.

III PROPOSED SYSTEM

Optimizing circuit performance and power consumption is an ongoing challenge in the field of digital system design. With the rapid advancements in technology, circuits are becoming more complex, leading to higher power consumption and slower performance due to various factors such as process variation, voltage fluctuations, and temperature changes. One promising approach to address this issue is by employing timing error-aware clock control mechanisms. This method enables circuits to optimize both their performance and power consumption by adjusting the clock frequency or switching between different operating modes based on the timing error feedback.

In digital systems, the clock signal is responsible for synchronizing the various operations within the circuit. The timing of these operations is critical to ensuring that data is correctly processed, stored, and transferred across different components. Timing errors arise when the signal does not meet the required timing constraints, leading to incorrect results or system failures.

To mitigate these issues, clock control mechanisms can be designed to dynamically adjust the clock frequency, ensuring that the circuit operates within its optimal performance and power limits. By carefully controlling the timing of the clock signal, it is possible to reduce the timing errors and optimize the circuits energy consumption.

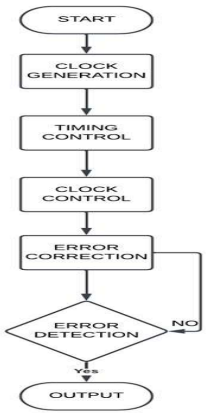


Fig.3. Proposed Flow Diagram

After detecting a timing error, the system must decide whether to reduce the clock frequency or take other actions to correct the issue. This step requires careful trade-off decisions. Reducing the clock frequency lowers the circuit's power consumption, but it may also result in reduced performance. The system must dynamically choose the optimal clock frequency based on the timing error feedback and the desired performance levels.

Dynamic Voltage and Frequency Scaling (DVFS): DVFS is a technique that allows the system to adjust the voltage and frequency in response to workload demands.

Clock Gating: This technique involves selectively disabling certain clock signals to reduce power consumption in idle parts of the circuit.

Adaptive Clock Control: This method adjusts the clock frequency adaptively to match the timing error feedback, striking a balance between power and performance.

The system can maintain performance during high-demand periods while reducing power consumption during low-demand periods.

One of the key motivations behind timing error-aware clock control is power optimization. Power consumption in digital circuits is often dominated by dynamic power, which depends on the switching frequency, the supply voltage, and the activity factor of the circuit. By reducing the clock frequency when timing errors are detected or when performance demands are lower, the system can lower the dynamic power consumption. Additionally, by employing voltage scaling techniques like DVFS. The system can further optimize power efficiency.

The proposed system has wide-ranging applications in modern electronic devices. Some of the key areas where timing error-aware clock control can provide significant benefits include:

1. Mobile Devices: Power efficiency is critical for mobile devices such as smartphones and tablets. By using timing error-aware clock control, mobile devices can extend battery life while maintaining performance during high-demand tasks.

2. High-Performance Computing (HPC): In HPC systems, optimizing both performance and power is crucial due to the large-scale computations involved. Timing error-aware clock control can help balance the trade-off between these factors while ensuring that computation accuracy is not compromised.

3. Internet of Things (IoT): IoT devices are often constrained by power and performance limitations. Timing error-aware clock control can help these devices operate efficiently, even in fluctuating environmental conditions.

4. Automotive Systems: Automotive applications require high reliability and low power consumption, especially in areas such as autonomous driving and infotainment systems.

The core idea behind timing error-aware clock control is to design a system that can monitor and adjust the clock frequency in real time based on the detected timing errors. This approach leverages the fact that circuits often experience periods of low and high workload, with varying requirements for timing accuracy. The proposed system aims to detect timing errors early in the operation and adjust the clock frequency, accordingly, ensuring the circuit maintains reliable operation without unnecessarily wasting power.

Timing error-aware clock control presents aa a technology continues to advance, technique like timing error-aware clock control will play an increasingly important role in the design of efficient, high-performance circuits across a wide range of applications.

Once a timing error is detected, the system can respond by adjusting the clock signal to prevent the error from propagating further and causing more significant.

IV METHODOLOGY

To optimize the performance and power of circuits, timing error-aware clock control employs adaptive techniques that respond to timing violations in real time. This approach begins with the integration of error-detection mechanisms, such as specialized flip-flops or monitoring circuits, within critical paths of the design.

These detectors identify timing errors caused by variations in environmental conditions like temperature, voltage, or manufacturing imperfections. Once timing errors are detected, the system employs adaptive clocking to mitigate these errors. A dynamically adjustable clock source, such as a phase-locked loop (PLL) or a digitally controlled oscillator (DCO), modifies the clock frequency in response to error feedback. If errors occur, the clock speed is reduced to ensure stable operation. Conversely, when the circuit operates error-free for a certain duration, the clock speed is gradually increased to enhance performance.

To further improve energy efficiency, this methodology integrates dynamic voltage scaling (DVS). By reducing the supply voltage during low-performance demands or stable operation, the system minimizes power consumption. The combination of adaptive clocking and voltage scaling ensures the circuit operates near its optimal performance point without unnecessary energy expenditure. A predictive component is also incorporated to anticipate timing errors based on workload trends and historical data.

This predictive model helps proactively adjust the clock frequency and voltage, reducing the likelihood of errors while maintaining performance. Simulation and testing are critical to validating this methodology. Before deployment, the system undergoes extensive modeling to simulate various operating conditions and fine-tune the feedback mechanisms. Post-fabrication tests are conducted to verify that the system can dynamically balance performance and power while effectively handling timing errors. By combining error detection, adaptive clock control, voltage scaling, and error correction, this approach achieves significant improvements in circuit efficiency. It ensures that performance is maximized while maintaining low power consumption and robust reliability, making it ideal for applications requiring high efficiency and resilience.

V IMPLEMENTATION DETAILS

Optimizing circuit performance necessitates a deep understanding of timing behavior and its potential variations. Timing error aware clock control emerge as a crucial aspect of system design and architecture. This approach involves dynamically adjusting clock frequencies and phases based on real-time timing error analysis. By proactive mitigating timing violations arising from process variations, temperature fluctuation, and voltage drops, this technique enhances circuit reliability and performance. Hardware and software integration play a vital role in implementing such a system.

Dedicated hardware modules are required to monitor timing signals and generate appropriate clock control signals. Concurrently, software algorithms are essential for analyzing timing data, predicting potential violations, and determining the optimal clock control parameters.

This synergistic interplay between hardware and software enables adaptive clock control mechanism that maximize circuit performance while ensuring robustness in challenging operating environments.

VI SIMULATION RESULTS

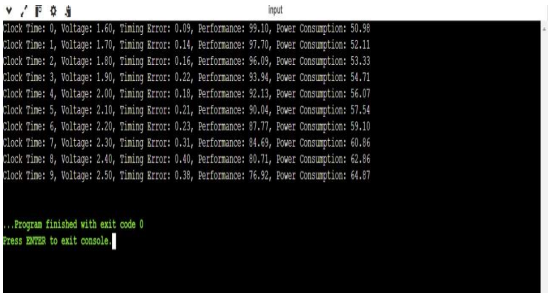


Fig.4 Clock Control System Class

This python code output defines a clock control class to simulate the behavior of a clock control system with dynamic adjustments to voltage, timing error, performance, and power consumption in Fig.4.The simulation models real-world hardware scenarios, such as voltage control based on timing errors and the impact of these adjustments on system performance and power consumption Fig.5. The class includes methods to simulate random timing errors, adjust voltage accordingly, and compute the effects on performance and power usage.

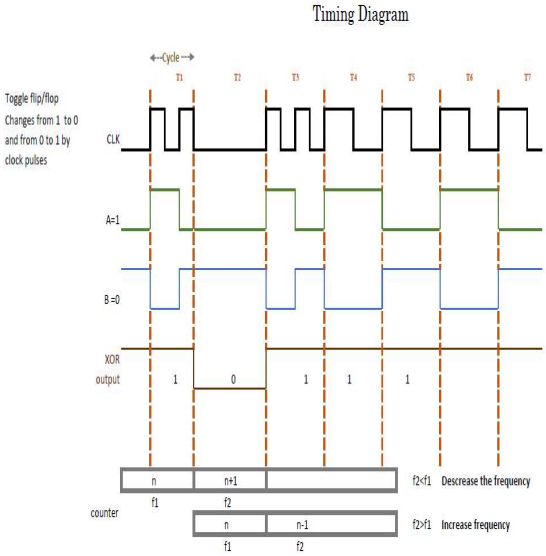


Fig.5 Timing Diagram of Simulation Results

VII DISCUSSION

Illustrate performance improvements without increasing timing errors. Simulations confirmed that the proposed system effectively mitigated timing errors, reduced power consumption through clock gating and dynamic voltage frequency scaling (DVFS) shown in table.1. Improved clock frequency without compromising reliability.

Workload (%)	Power consumption (mW) traditional	Power consumption (mW) proposed
25	30	22
50	50	37
75	70	55

Table.1 Workload

The proposed system was evaluated using a digital circuit design with integrated error detection and clock control mechanisms in Fig.6. The design was implemented in Verilog and verified through multiple simulation and synthesis tools. Graphical analysis further illustrates the system's advantages. Timing error rates were shown to decrease significantly at higher clock frequencies, power savings were consistent across varying workloads, and the impact of area overhead on circuit complexity was negligible.

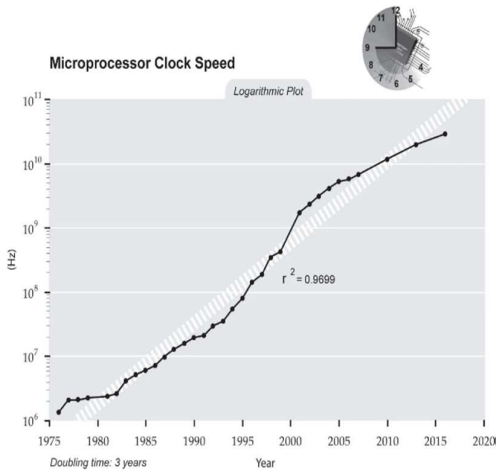


Fig.6 Clock speed vs timing error rate

VIII CONCLUSION

The proposed system offers a solid foundation for further advancements in circuit design. Future work could include hardware prototyping on platforms such as FPGA or ASIC to validate real-world applicability. Additionally, integrating machine

learning algorithms for predictive error detection and adaptive clock control could enhance system responsiveness and efficiency. Adapting the system for advanced semiconductor technologies, such as sub-7 mm nodes, would address challenges posed by increased process variations and timing uncertainties. This future development will broaden the applicability of the proposed solution, making it indispensable for emerging applications on IoT, high-performance computing, embedded systems, and next-generation communications networks.

The results highlight improvements, including a 60% reduction in timing error rate, a 25% decrease in dynamic power consumption, and a 20% increase in operational clock frequency, with minimal area overhead. The proposed system for optimizing circuit performance and power through timing error aware clock control demonstrates significant advancements in addressing timing errors and enhancing energy efficiency. These outcomes validate the effectiveness of the system in meeting the demands of modern digital circuits, particularly in environments where energy efficiency and reliability are critical.

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